WHAT IS CLAIMED IS:

1. An echo canceller, for an asymmetric communication system, comprising :

a delay line block for delaying an echo input signal for a predetermined interval to generate a delay signal;

a filter coefficient table block for sequentially shifting filter coefficients stored in a shift register, and for outputting a filter coefficient; and

a multiplication and accumulation block for multiplying and adding the delay signal of the delay line block by the filter coefficient output by the filter coefficient table block to generate an echo-cancelled echo output signal.

2. The echo canceller of claim 1, wherein the echo canceller is a finite impulse response (FIR) filter that calculates the correlativity between the echo input signal and an echo output signal to generate the filter coefficients.

3. The echo canceller of claim 1, wherein the shift register is used in a central office (CO) mode and in an remote terminal (RT) mode of the asymmetric communication system.

4. The echo canceller of claim 1, wherein the filter coefficient output by the filter coefficient table block has a shift rate of 1:4.

5. The asymmetric communication system of claim 1, wherein the delay line block divides a line for inputting the echo input signal into eight delay lines to delay the echo input signal.

6. An asymmetric communication system, having an echo canceller, that includes:

an input interface block for receiving echo input data of a first rate in a first mode and echo input data of a second rate in an second mode;

a sub FIFO block for shifting the echo input data of the first rate in the first mode by downsampling and shifting the echo input data of the second rate in the second mode by upsampling;

a main FIFO block for shifting the echo input data of the second rate in the first mode and shifting the echo input data of the first rate in the second mode;

a multiplexer for selectively connecting the sub FIFO block to the main FIFO block; and

an input interface block for generating an echo output signal of the second rate in the first mode and generating an echo output signal of the first rate in the second mode.

7. The asymmetric communication system of claim 6, wherein the input interface block, the sub FIFO block, the main FIFO block, and the output interface block are sequentially connected in the first mode; and wherein

the input interface block, the main FIFO block, the sub FIFO block, and the output interface block are sequentially connected in the second mode.

8. The asymmetric communication system of claim 6, wherein the echo canceller further includes a multiplication and accumulation block for multiplying and adding the filter coefficient stored in the sub FIFO block in the first mode by the filter coefficient stored in the main FIFO block.

9. The asymmetric communication system of claim 6, wherein the main FIFO block mainly delays the echo input signal.

10. The asymmetric communication system of claim 6, wherein the sub FIFO block finely delays the echo input signal.

11. The asymmetric communication system of claim 6, wherein the main FIFO block is a 128-depth FIFO and the sub FIFO block is a four-depth FIFO.

12. The asymmetric communication system of claim 6, wherein the echo canceller operates relative to an echo-dominant channel among channels of the asymmetric communication system.

13. The asymmetric communication system of claim 12, wherein the echo canceller receives the delay of the echo-dominant channel from a digital signal processor (DSP).

14. A method for downloading a filter coefficient of an echo canceller in an asymmetric communication system, the method comprising the steps of:

(*a*) performing an echo cancel training for a newly generated loop during an initial period to determine a filter coefficient;

(*b*) comparing a write register value with a read register value

and writing the filter coefficient into a data register and toggling the write register value when the write register value and the read register value are identical to each other;

(*c*) repeatedly performing the steps (*a*) and (*b*) while a first index increases;

(*d*) comparing the read register value and the write register value with each other, in response to a second value of the download register, and writing the coefficient stored in the data register to a shift register in the echo canceller when the read and write register values are the same;

(*e*) sequentially shifting the shift register to toggle the read register value.

15. The method of claim 14, wherein the steps of (*a*) to (*c*) are performed by a digital signal processor (DSP).

16. The method of claim 14, wherein the steps of (*d*) to (*f*) are performed by the echo canceller.

17. method of claim 16, wherein the echo canceller includes a multiplication and accumulation block for multiplying and adding a stored filter coefficient.